Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application. Please cancel claim 1, and add new claims 47-80, as follows:

Listing of Claims:

1-46. (Cancelled)

47. (New) An input stage for generating an output signal having a voltage level according to the voltage level of an input signal relative to a reference voltage level, the input stage comprising:

an input buffer circuit having an input node at which the input signal is applied, a reference node at which a reference voltage signal having the reference voltage level is applied, and an output node at which the output signal is provided;

an amplifier circuit having an input node to which a standard reference voltage signal is applied, a first output node at which a first reference voltage signal generated by the amplifier circuit and having a first voltage level greater than the standard reference voltage signal is provided, and further having a second output node at which a second reference voltage signal generated by the amplifier circuit and having a second voltage level less than the standard reference voltage signal is provided; and

a multiplexer having a selection terminal coupled to the output node of the input buffer, an output coupled to the reference node, and first and second input terminals coupled to the first and second output nodes of the amplifier, respectively, the multiplexer coupling the first reference voltage signal to the reference node in response to the output signal of the input buffer having a low logic level and coupling the second reference voltage signal to the reference node in response to the output signal of the input buffer having a high logic level.

48. (New) The input stage of claim 47 wherein the amplifier circuit comprises:

a differential amplifier having a first input at which the input signal is applied, a second input and an output; and

a voltage divider circuit having an input, a first node, a second node and a third node at which different voltage levels are coupled, the input node of the voltage divider circuit coupled to the output of the differential amplifier, the first node coupled to the first input terminal of the multiplexer, the second node coupled to the second input of the differential amplifier, and the third node coupled to the second input terminal of the multiplexer.

49. (New) The input stage of claim 48 wherein the voltage divider circuit comprises:

a first resistor coupled between the input and the first node;

a second resistor coupled between the first node and the second node;

a third resistor coupled between the second node and third node; and

a fourth resistor coupled between the third node and ground.

50. (New) The input stage of claim 47, further comprising:

a first capacitor having a first node coupled to the first output node of the amplifier circuit and a second node to which the reference voltage signal is applied; and

a second capacitor having a first node coupled to the second output node of the amplifier circuit and a second node coupled to the second node of the first capacitor.

51. (New) The input stage of claim 47 wherein the multiplexer comprises:

a first transfer gate having an input coupled to the first output node of the amplifier circuit and an output coupled to the input node of the input buffer, the first transfer gate having a control terminal coupled to the output node of the input buffer; and

a second transfer gate having an input coupled to the second output node of the amplifier circuit and an output coupled to the input node of the input buffer, the second transfer gate having a control terminal coupled to the output node off the input buffer.

52. (New) An input stage, comprising:

a differential amplifier having first and second input nodes and an output node, a standard reference signal having a standard reference voltage applied to the first input node;

first, second, third, and fourth series coupled resistors having a first node between the first and second resistors, a second node between the second and third resistors and a third node between the third and fourth resistors, the series coupled resistors coupled between the output node of the differential amplifier and ground, the second node coupled to the second input node of the differential amplifier;

an input buffer circuit having an input node, a reference node and an output node, the input buffer generating an output signal having a voltage level according to the voltage level of an input signal applied to the first input node relative to the voltage level of a reference signal applied to the reference node;

a first switch coupled to the first node of the series coupled resistors and the reference node and having a control node coupled to the output of the input buffer, the first switch coupling the first node and the reference node together in response to an output signal having a voltage level less than the standard reference signal; and

a second switch coupled to the third node of the series coupled resistors and the reference node and having a control node coupled to the output of the input buffer, the second switch coupling the third node and the reference node together in response to an output signal having a voltage level greater than the standard reference signal.

53. (New) The input stage of claim 52 wherein the first switch comprises a first transfer gate and the second switch comprises a second transfer gate.

54. (New) The input stage of claim 52 wherein the first and second switches are included in a multiplexer.

55. (New) The input stage of claim 52, further comprising:

a first capacitor having a first node coupled to the first node of the series coupled resistors and a second node to which the standard reference signal is applied; and

a second capacitor having a first node coupled to the third node of the series coupled resistors and a second node coupled to the second node of the first capacitor.

56. (New) The input stage of claim 52 wherein the input buffer comprises a SSTL input buffer.

57. (New) A memory device, comprising:

an address bus;

a control bus;

a data bus;

an address decoder coupled to the address bus;

a read/write circuit coupled to the data bus;

a memory-cell array coupled to the address decoder, control circuit, and read/write circuit; and

an input stage for providing an output signal having a logic value based on the voltage of an input signal, the input stage comprising:

an input buffer having an input terminal to which the input signal is applied, an output terminal at which the output signal is provided, and a reference terminal to which a reference voltage signal is applied, the input buffer generating an output signal having a logic value based on the voltage of the input signal relative to the voltage of the reference voltage signal;

an operational amplifier having a first input at which an initial reference voltage is applied, a second input, and an output;

a voltage divider circuit coupled between the output of the operational amplifier and a reference voltage supply, the voltage divider circuit having a first node at which a high reference voltage is provided, a second node coupled to the second input of the operational amplifier, and a third node at which a low reference voltage is provided; and

first and second transfer gates coupled to the first and second nodes of the voltage divider, respectively, each transfer gate having control terminals to which the output of the input buffer is coupled, the first transfer gate coupling the high reference voltage signal to the reference terminal in response to the output signal of the input buffer having a low logic value and the second transfer gate coupling the low reference voltage signal to the reference terminal in response to the output signal of the input buffer having a high logic value.

58. (New) The memory device of claim 57 wherein the input stage further comprises a first capacitor having a first terminal coupled to the first node and a second capacitor having a first terminal coupled to the third node, the first and second capacitors each having a second terminal to which the initial reference voltage signal is applied.

59. (New) The memory device of claim 57 wherein the voltage divider of the input stage comprises:

a first resistor electrically coupled between the output of the operational amplifier and the first node;

a second resistor electrically coupled between the first node and the second node;

a third resistor electrically coupled between the second node and the third node; and

a fourth resistor electrically coupled between the third node and the reference voltage supply.

60. (New) The memory device of claim 57 wherein the input stage further comprises first and second transfer gates coupled to the first and second output terminals of the amplifier, respectively, each transfer gate having control terminals to which the output of the

input buffer is coupled, the first transfer gate coupling the high reference voltage signal to the reference terminal in response to the output signal of the input buffer having a low logic value and the second transfer gate coupling the low reference voltage signal to the reference terminal in response to the output signal of the input buffer having a high logic value.

61. (New) A memory device, comprising:

an address bus;

a control bus;

a data bus;

an address decoder coupled to the address bus;

a read/write circuit coupled to the data bus;

a memory-cell array coupled to the address decoder, control circuit, and read/write circuit; and

an input stage including an SSTL input buffer having input signal terminal, an output terminal and a reference voltage terminal, the input stage comprising:

an amplifier having an input to which a initial reference voltage signal is applied and further having first and second output terminals, the amplifier generating from the initial reference voltage signal a high reference voltage signal at the first output terminal and a low reference voltage signal at the second output terminal; and

a selection circuit having first and second input terminals coupled to the first and second output terminals of the amplifier, respectively, an output terminal coupled to the reference voltage terminal, and a control terminal coupled to the output terminal of the input buffer, the selection circuit selectively coupling the first and second input terminals to the output terminal based on a logic value of an output signal of the input buffer to provide either the high or low reference voltage signals to the input buffer as the reference voltage signal.

62. (New) The memory device of claim 61 wherein the amplifier of the input stage comprises:

an operational amplifier having a first input at which the initial reference voltage is applied, a second input, and an output at which an output signal is provided; and

a voltage divider circuit coupled between the output of the operational amplifier and a reference voltage supply, the voltage divider circuit having a first node at which the high reference voltage signal is provided, a second node coupled to the second input of the operational amplifier, and a third node at which the low reference voltage signal is provided.

63. (New) The memory device of claim 62 wherein the voltage divider of the input stage comprises:

a first resistor electrically coupled between the output of the operational amplifier and the first node;

a second resistor electrically coupled between the first node and the second node;

a third resistor electrically coupled between the second node and the third node; and

a fourth resistor electrically coupled between the third node and the reference voltage supply.

64. (New) The memory device of claim 61 wherein the selection circuit of the input stage comprises a multiplexer having a selection terminal coupled to the output terminal of the input buffer, an output coupled to the reference terminal, and first and second input terminals coupled to the first and second output terminals of the amplifier, respectively, the multiplexer providing the high reference voltage signal as the reference voltage signal in response to the output signal of the input buffer having a low logic value and the low reference voltage signal as the reference voltage signal in response to the output signal of the input buffer having a high logic value.

65. (New) The memory device of claim 61 wherein the selection circuit of the input stage comprises first and second transfer gates coupled to the first and second output terminals of the amplifier, respectively, each transfer gate having control terminals to which the output of the input buffer is coupled, the first transfer gate coupling the high reference voltage signal to the reference terminal in response to the output signal of the input buffer having a low logic value and the second transfer gate coupling the low reference voltage signal to the reference terminal in response to the output signal of the input buffer having a high logic value.

66. (New) The memory device of claim 61 wherein the input stage further comprises a first capacitor having a first terminal coupled to the first node and a second capacitor having a first terminal coupled to the third node, the first and second capacitors each having a second terminal to which the initial reference voltage signal is applied.

67. (New) A memory device, comprising:

an address bus;

a control bus;

a data bus;

an address decoder coupled to the address bus;

a read/write circuit coupled to the data bus;

a memory-cell array coupled to the address decoder, control circuit, and read/write circuit; and

an input stage for generating an output signal having a voltage level according to the voltage level of an input signal relative to a reference voltage level, the input stage comprising:

an input buffer circuit having an input node at which the input signal is applied, a reference node at which a reference voltage signal having the reference voltage level is applied, and an output node at which the output signal is provided;

an amplifier circuit having an input node to which a standard reference voltage signal is applied, a first output node at which a first reference voltage signal generated by

the amplifier circuit and having a first voltage level greater than the standard reference voltage signal is provided, and further having a second output node at which a second reference voltage signal generated by the amplifier circuit and having a second voltage level less than the standard reference voltage signal is provided; and

a multiplexer having a selection terminal coupled to the output node of the input buffer, an output coupled to the reference node, and first and second input terminals coupled to the first and second output nodes of the amplifier, respectively, the multiplexer coupling the first reference voltage signal to the reference node in response to the output signal of the input buffer having a low logic level and coupling the second reference voltage signal to the reference node in response to the output signal of the input buffer having a high logic level.

68. (New) The memory device of claim 67 wherein the amplifier circuit of the input stage comprises:

a differential amplifier having a first input at which the input signal is applied, a second input and an output; and

a voltage divider circuit having an input, a first node, a second node and a third node at which different voltage levels are coupled, the input node of the voltage divider circuit coupled to the output of the differential amplifier, the first node coupled to the first input terminal of the multiplexer, the second node coupled to the second input of the differential amplifier, and the third node coupled to the second input terminal of the multiplexer.

69. (New) The memory device of claim 68 wherein the voltage divider circuit of the input stage comprises:

a first resistor coupled between the input and the first node;

a second resistor coupled between the first node and the second node;

a third resistor coupled between the second node and third node; and

a fourth resistor coupled between the third node and ground.

70. (New) The memory device of claim 67 wherein the input stage further comprises:

a first capacitor having a first node coupled to the first output node of the amplifier circuit and a second node to which the reference voltage signal is applied; and

a second capacitor having a first node coupled to the second output node of the amplifier circuit and a second node coupled to the second node of the first capacitor.

71. (New) The memory device of claim 67 wherein the multiplexer of the input stage comprises:

a first transfer gate having an input coupled to the first output node of the amplifier circuit and an output coupled to the input node of the input buffer, the first transfer gate having a control terminal coupled to the output node of the input buffer; and

a second transfer gate having an input coupled to the second output node of the amplifier circuit and an output coupled to the input node of the input buffer, the second transfer gate having a control terminal coupled to the output node off the input buffer.

72. (New) A memory device, comprising:

an address bus;

a control bus;

a data bus;

an address decoder coupled to the address bus;

a read/write circuit coupled to the data bus;

a memory-cell array coupled to the address decoder, control circuit, and read/write circuit; and

an input stage, comprising:

a differential amplifier having first and second input nodes and an output node, a standard reference signal having a standard reference voltage applied to the first input node;

first, second, third, and fourth series coupled resistors having a first node between the first and second resistors, a second node between the second and third resistors and a third node between the third and fourth resistors, the series coupled resistors coupled between the output node of the differential amplifier and ground, the second node coupled to the second input node of the differential amplifier;

an input buffer circuit having an input node, a reference node and an output node, the input buffer generating an output signal having a voltage level according to the voltage level of an input signal applied to the first input node relative to the voltage level of a reference signal applied to the reference node;

a first switch coupled to the first node of the series coupled resistors and the reference node and having a control node coupled to the output of the input buffer, the first switch coupling the first node and the reference node together in response to an output signal having a voltage level less than the standard reference signal; and

a second switch coupled to the third node of the series coupled resistors and the reference node and having a control node coupled to the output of the input buffer, the second switch coupling the third node and the reference node together in response to an output signal having a voltage level greater than the standard reference signal.

73. (New) The memory device of claim 72 wherein the first switch of the input stage comprises a first transfer gate and the second switch of the input stage comprises a second transfer gate.

74. (New) The memory device of claim 72 wherein the first and second switches of the input stage are included in a multiplexer.

75. (New) The memory device of claim 72 wherein the input stage further comprises:

a first capacitor having a first node coupled to the first node of the series coupled resistors and a second node to which the standard reference signal is applied; and

a second capacitor having a first node coupled to the third node of the series coupled resistors and a second node coupled to the second node of the first capacitor.

76. (New) The memory device of claim 72 wherein the input buffer of the input stage comprises a SSTL input buffer.

77. (New) A computer system, comprising:

a data input device;

a data output device;

a processor coupled to the data input and output devices; and

a memory device coupled to the processor, the memory device comprising:

an address bus;

a control bus;

a data bus;

an address decoder coupled to the address bus;

a read/write circuit coupled to the data bus;

a memory-cell array coupled to the address decoder, control circuit, and read/write circuit; and

an input stage for providing an output signal having a logic value based on the voltage of an input signal, the input stage comprising:

an input buffer having an input terminal to which the input signal is applied, an output terminal at which the output signal is provided, and a reference terminal to which a reference voltage signal is applied, the input buffer generating an output signal having a logic value based on the voltage of the input signal relative to the voltage of the reference voltage signal;

an operational amplifier having a first input at which an initial reference voltage is applied, a second input, and an output;

a voltage divider circuit coupled between the output of the operational amplifier and a reference voltage supply, the voltage divider circuit having a first

node at which a high reference voltage is provided, a second node coupled to the second input of the operational amplifier, and a third node at which a low reference voltage is provided; and

first and second transfer gates coupled to the first and second nodes of the voltage divider, respectively, each transfer gate having control terminals to which the output of the input buffer is coupled, the first transfer gate coupling the high reference voltage signal to the reference terminal in response to the output signal of the input buffer having a low logic value and the second transfer gate coupling the low reference voltage signal to the reference terminal in response to the output signal of the input buffer having a high logic value.

78. (New) A computer system, comprising:

a data input device;

a data output device;

a processor coupled to the data input and output devices; and

a memory device coupled to the processor, the memory device comprising:

an address bus;

a control bus;

a data bus;

an address decoder coupled to the address bus;

a read/write circuit coupled to the data bus;

a memory-cell array coupled to the address decoder, control circuit, and read/write circuit; and

an input stage including an SSTL input buffer having input signal terminal, an output terminal and a reference voltage terminal, the input stage comprising:

an amplifier having an input to which a initial reference voltage signal is applied and further having first and second output terminals, the amplifier generating from the initial reference voltage signal a high reference voltage signal at the first output terminal and a low reference voltage signal at the second output terminal; and

a selection circuit having first and second input terminals coupled to the first and second output terminals of the amplifier, respectively, an output terminal coupled

to the reference voltage terminal, and a control terminal coupled to the output terminal of the input buffer, the selection circuit selectively coupling the first and second input terminals to the output terminal based on a logic value of an output signal of the input buffer to provide either the high or low reference voltage signals to the input buffer as the reference voltage signal.

79. (New) A computer system, comprising:

a data input device;

a data output device;

a processor coupled to the data input and output devices; and

a memory device coupled to the processor, the memory device comprising:

an address bus;

a control bus;

a data bus;

an address decoder coupled to the address bus;

a read/write circuit coupled to the data bus;

a memory-cell array coupled to the address decoder, control circuit, and read/write circuit; and

an input stage for generating an output signal having a voltage level according to the voltage level of an input signal relative to a reference voltage level, the input stage comprising:

an input buffer circuit having an input node at which the input signal is applied, a reference node at which a reference voltage signal having the reference voltage level is applied, and an output node at which the output signal is provided;

an amplifier circuit having an input node to which a standard reference voltage signal is applied, a first output node at which a first reference voltage signal generated by the amplifier circuit and having a first voltage level greater than the standard reference voltage signal is provided, and further having a second output node at which a second reference voltage signal generated by the amplifier circuit and having a second voltage level less than the standard reference voltage signal is provided; and

a multiplexer having a selection terminal coupled to the output node of the input buffer, an output coupled to the reference node, and first and second input terminals coupled to the first and second output nodes of the amplifier, respectively, the multiplexer coupling the first reference voltage signal to the reference node in response to the output signal of the input buffer having a low logic level and coupling the second reference voltage signal to the reference node in response to the output signal of the input buffer having a high logic level.

80. (New) A computer system, comprising:

a data input device;

a data output device;

a processor coupled to the data input and output devices; and

a memory device coupled to the processor, the memory device comprising:

an address bus;

a control bus;

a data bus;

an address decoder coupled to the address bus;

a read/write circuit coupled to the data bus;

a memory-cell array coupled to the address decoder, control circuit, and read/write circuit; and

an input stage, comprising:

a differential amplifier having first and second input nodes and an output node, a standard reference signal having a standard reference voltage applied to the first input node;

first, second, third, and fourth series coupled resistors having a first node between the first and second resistors, a second node between the second and third resistors and a third node between the third and fourth resistors, the series coupled resistors coupled between the output node of the differential amplifier and ground, the second node coupled to the second input node of the differential amplifier;

an input buffer circuit having an input node, a reference node and an output node, the input buffer generating an output signal having a voltage level according to the voltage level of an input signal applied to the first input node relative to the voltage level of a reference signal applied to the reference node;

a first switch coupled to the first node of the series coupled resistors and the reference node and having a control node coupled to the output of the input buffer, the first switch coupling the first node and the reference node together in response to an output signal having a voltage level less than the standard reference signal; and

a second switch coupled to the third node of the series coupled resistors and the reference node and having a control node coupled to the output of the input buffer, the second switch coupling the third node and the reference node together in response to an output signal having a voltage level greater than the standard reference signal.